REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action January 7, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-26 are under consideration in this application. Claims 1-6 and 8-26 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention.

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

The claims were objected to for various formal errors, and claim 12 was rejected under 35 U.S.C. §112, second paragraph, for language that lacked proper antecedent basis.

As indicated, the claims are being amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejections is in order, and is therefore respectfully solicited.

Allowed Subject Matters

Claims 7 and 14 would be allowed if they are rewritten in independent form to include the limitations of the base claim and any intervening claims.

Prior Art Rejections

Claims 1 – 5 and 8 - 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 6,665,802 to Ober (hereinafter "Ober") in view of the admitted prior art discussed in the specification (hereinafter "AAPA"), claims 6, 12, 13 and 15-26 were rejected under 35 U.S.C. §103(a) on the grounds of being unpatentable over Ober and AAPA, in view of US Patent

No. 6,266,776 to Sakai (hereinafter "Sakai"). US Patent No. 6,754,837 to Helms was cited as being pertinent to the disclosure of the present invention. These rejections are being carefully considered in view of claim 3-6, but are most respectfully traversed as follows.

The data processor 1 (for example, the embodiment depicted in Fig. 1) of the invention comprises a CPU 2, a clock pulse generator 3 (including a frequency driver 40 and a PLL circuit 41 therein; Fig. 2; see Pat. App. Pub. No. US 2002-0073352 Paragraph [0033]) and a plurality of other circuit modules (i.e., circuits other than the CPU 2 and the clock pulse generator 3, e.g., a mode control circuit 4, a timer 5, a interrupt control circuit 6, a built-in peripheral circuit 7, etc.). The data processor has a plurality operation modes (Fig. 5) including a program running mode ST1, a sleep mode ST2 (a first mode), a light standby mode ST3 (a second mode), and a standby mode ST4. In the program running mode ST1, the CPU 2 is capable of executing a plurality of instructions ([0042]). In the sleep mode ST2, the clock pulse generator 3 generates clock signals, while the CPU 2 is not supplied with any clock signal and the other circuit modules are supplied with the clock signals from the clock pulse generator 3 ([0010],[0037]). In the light standby mode ST3, the clock pulse generator 3 generates clock signals, while the CPU 2 and other circuit modules are not supplies with the clock signals ([0010], [0045]). In the standby mode ST4, the clock pulse generator 3 stops generating any clock signal such that there is no clock signal supplied to the CPU 2 and other circuit modules ([0010], [0037]). In summary:

	Operation of clock pulse generator 3	Clock to central processing unit 2	Clock to other circuit modules
Program Running mode	operate	Supply	Supply
Sleep/1st mode	operate	Not supply	supply
Light standby/2nd mode	**operate**	**Not supply**	**Not supply**
Standby mode	Not operate	Not supply	Not supply

Claim 1 recites a data processor operating under all four modes, and claim 12 recites a data processor operating under three out of the four modes (except the Standby mode ST4). Claim 24 recites a data processing system including the data processor of claim 1, a memory which is accessed by the central processing unit of the data processor, and a circuit that requests an interrupt to the data processor. Claim 26 recites the data processing system of claim 24, wherein the mode control circuit includes a control register, and sets the first mode in response to a first state of the control register when a predetermined instruction is executed by the central

processing unit, and sets the second mode in response to a second state of the control register when a predetermined instruction is executed by the central processing unit.

Applicants respectfully contend that none of the cited prior art references teaches or suggests such "a light standby mode (claim 1) or a second mode (claim 12) in which the clock pulse generator operates the frequency multiplication and frequency division operation, but stops supplying clock signals to a CPU and other circuit modules" according the invention.

In contrast, Ober's "SLEEP MODE (*Clock Distributed*)" (p. 4, lines 1-3 of the outstanding Office Action), which relied upon by the examiner to teach the light standby mode of the invention, stops supplying "*the clock for CPU 22 and selected peripheral clocks [is stopped] to reduce power consumption while waiting for internal or external interrupt events* (col. 15, lines 46-48)," at the same time "***all other on-chip clocks, PLL's and devices not explicitly stopped by program control function normally*** (col. 15, lines 53-55)." In other words, Ober not only sends clock signals to circuit modules for the frequency multiplication and frequency division operation (as asserted by the Examiner on p. 4, lines 1-8 of the outstanding Office Action), but also sends clock signals to circuit modules NOT for the frequency multiplication and frequency division operation such as "*the subsystems which have been preconfigured to operate in the SLEEP mode* (in col. 13, Table 9 4th and 5th lines from the bottom)". These subsystems include memory, ICU, RTC, Watchdog, Power, Management, Reset, Pins, FPI Bus, etc (col. 13, Table 8, under "Units Clocked" heading and in "SLEEP MODE (*Clock Distributed*)"). As such, Ober's "SLEEP MODE (*Clock Distributed*)" does NOT stop supplying clock signals to "other circuit modules" of the invention i.e., circuits other than the CPU2 and the clock pulse generator 3, e.g., a mode control circuit 4, a timer 5, an *interrupt* control circuit 6, a built-in peripheral circuit 7, etc. according to the invention. Accordingly, Ober's "SLEEP MODE (*Clock Distributed*)" operates differently from the light standby mode of the invention.

AAPA and Sakai fail to compensate for Ober's deficiencies. AAPA only teaches a frequency multiplication in a clock pulse generator, and Sakai only teaches a timer system used to determine when to change power modes.

Accordingly, Applicants contend that the cited references do not embody each and every feature of the present invention as now claimed in claims 1, 12, 24 and 26. The difference is more than sufficient that the present invention as now claimed would not have been anticipated

or rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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